

WHAT IS CLAIMED IS:

1. An electrical interconnect structure on a substrate,
comprising:
 - 5 a first low k or ultra low k dielectric layer;
a low k CMP protective layer disposed on said first low k dielectric
layer; and
a CVD hardmask/CMP polish stop layer.
- 10 2. The electrical interconnect structure of claim 1, wherein said
first low k dielectric layer is a first spin-on low k dielectric layer.
3. The electrical interconnect structure of claim 1, wherein said
first low k dielectric layer is comprised of an organic dielectric material.
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4. The electrical interconnect structure of claim 2, wherein said
spin-on low k dielectric layer is selected from the group consisting of:
SiLK™, GX-3™, porous SiLK™, GX-3p™, JSR LKD 5109™, porous spin-
on Si_wC_xO_yH_z material, spin-on dielectric material, low k spin-on dielectric
20 material and porous low k spin-on dielectric material.
5. The electrical interconnect structure of claim 1, wherein said
low k CMP protective layer is a spin-on low k CMP protective layer.
- 25 6. The electrical interconnect structure of claim 1, wherein said
low k CMP protective layer is covalently bonded to said first low k
dielectric layer.
7. The electrical interconnect structure of claim 5, wherein said
30 spin-on low k CMP protective layer is comprised of a material with a low

CMP polish rate that can be directly polished without scratching or producing other defects.

8. The electrical interconnect structure of claim 5, wherein said spin-on low k CMP protective layer has a dielectric constant of from about 2.2 to about 3.5.

9. The electrical interconnect structure of claim 5, wherein said spin-on low k CMP protective layer is inert to chemicals contained in CMP polish slurries.

10. The electrical interconnect structure of claim 5, wherein said spin-on low k CMP protective layer has molecular level free volume or molecular level porosity.

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11. The electrical interconnect structure of claim 10, wherein said molecular level free volume has a size ranging from about 2 Å to about 50 Å.

12. The electrical interconnect structure of claim 10, wherein said molecular level porosity has a volume percent from about 5% to about 80%.

13. The electrical interconnect structure of claim 5, wherein said spin-on low k CMP protective layer mechanically behaves like a sponge, which provides damping capability under application of down force during polish.

14. The electrical interconnect structure of claim 5, wherein said spin-on low k CMP protective layer has fine and evenly dispersed pores.

15. The electrical interconnect structure of claim 5, wherein said CMP protective layer is comprised of a spin-on material selected from the group consisting of: HOSP™, AP 6000™, HOSP BEST™, Ensemble™ Etch Stop, Ensemble™ Hard Mask, organo silsesquioxane, hydrido silsesquioxane, hydrido-organo silsesquioxane copolymer, siloxane, and silsesquioxane.

16. The electrical interconnect structure of claim 15, wherein said spin-on material has a low dielectric constant and low CMP polish rate.

17. The electrical interconnect structure of claim 1, wherein said CVD hardmask/CMP polish stop layer is a conventional CVD hardmask/CMP polish stop layer.

18. The electrical interconnect structure of claim 17, wherein said hardmask / CMP polish stop layer is comprised of BLOk™, silicon nitride, silicon carbide, $\text{Si}_x\text{C}_y\text{N}_z$, and CVD deposited material with a low CMP polish rate.

19. The electrical interconnect structure of claim 1, wherein said first low-k dielectric is an organic dielectric, and said spin-on low k CMP protective layer is an inorganic material or an inorganic/organic hybrid material.

20. The electrical interconnect structure of claim 1, wherein said first low k dielectric is porous.

21. The electrical interconnect structure of claim 1, wherein said first low k dielectric is a stack of dielectric containing an embedded etch stop.

22. The interconnect structure of claim 1, wherein said first low k dielectric layer has a thickness of from about 600 Å to about 8000 Å.

5 23. The electrical interconnect structure of claim 1, wherein said spin-on low k CMP protective layer has a thickness from about 50 Å to about 500 Å.

24. The interconnect structure of claim 1 wherein said substrate
10 is a semiconductor wafer having an adhesion promoter layer formed thereon.

25. The electrical interconnect structure of claim 1, further comprising:
15 a stack of dielectric layers on said substrate, said stack including at least said first low-k dielectric layer and said spin-on low k CMP protective layer.

26. The electrical interconnect structure of claim 25, further
20 comprising: a plurality of patterned metal conductors formed within said stack of said first low-k dielectric layer and said spin-on low k CMP protective layer.

27. The electrical interconnect structure of claim 26, wherein at
25 least one of said patterned metal conductors is an electrical via.

28. The electrical interconnect structure of claim 27, wherein at
least one of said patterned metal conductors is a line connected to said
via.

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29. The electrical interconnect structure of claim 25, further comprising:

a single level of patterned metal conductors formed within said stack of dielectric layers on said substrate.

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30. The electrical interconnect structure of claim 29, wherein said patterned metal conductors is a line.

31. The electrical interconnect structure of claim 29, wherein
10 said patterned metal conductors is a via.

32. A method of forming an electrical interconnect structure on a substrate, comprising:

forming a low k CMP protective layer on a first low-k dielectric or an
15 ultra low k dielectric layer disposed on a substrate such that said CMP protective layer covalently bonds with said first low-k dielectric or said ultra low k dielectric layer; and

forming a hardmask/CMP polish stop layer on said low k CMP protective layer..

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33. The method of claim 32, wherein said first low-k dielectric layer is a first spin-on low k dielectric layer..

34. The method of claim 33, wherein said spin-on low k dielectric
25 layer is selected from the group consisting of: SiLK™, GX-3™, porous SiLK™, GX-3p™, JSR LKD 5109™, porous spin-on Si_wC_xO_yH_z material, spin-on dielectric material, low k spin-on dielectric material and porous low k spin-on dielectric material.

35. The method of claim 32, wherein said first low-k dielectric
30 layer is porous.

36. The method of claim 32, wherein said first low-k dielectric layer has a thickness from about 600 Å to about 8000 Å.

5 37. The method of claim 32, wherein said low-k CMP protective layer is a spin-on low-k CMP protective layer having a thickness from about 50 Å to about 500 Å.

38. The method of claim 32, wherein said CMP protective layer
10 is comprised of a spin-on material selected from the group consisting of: HOSP™, AP 6000™, HOSP BEST™, Ensemble™ Etch Stop, Ensemble™ Hard Mask, organo silsesquioxane, hydrido silsesquioxane, hydrido-organosilsesquioxane copolymer, siloxane and silsesquioxane.

15 39. The method of claim 32, further comprising:
forming a metal line in said first dielectric layer.

40. The method of claim 32, further comprising:
forming a metal via in said dielectric layer.

20 41. The method of claim 32, further comprising:
adding additional dielectric layers; and
adding conductors to complete said electrical interconnect structure.

25 42. The method of claim 41, further comprising:
forming a stack of dielectric layers on said substrate, including at least said first dielectric layer and said low k CMP protective layer; and
forming a plurality of patterned metal conductors within said
30 dielectric layers.

43. The method of claim 42, further comprising:
curing said dielectric layers to promote crosslinking of said CMP
protective layer to said first low k dielectric layer and to reduce CMP polish
rate of said CMP protective layer.

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44. The method of claim 43, wherein said first dielectric and said
CMP protective layers are cured in a single step.

45. The method of claim 44, wherein said first dielectric and said
10 CMP protective layers are cured in a furnace at a temperature from about
300°C to about 500°C within a period of time from about 15 minutes to
about 3 hours.

46. The method of claim 43, wherein said dielectric layers in said
15 stack are cured after sequential application in a single tool.

47. The method of claim 46, wherein said application tool is a
spin coating tool containing high temperature hot plate baking chambers.

20 48. The method of claim 32, wherein said first low k dielectric
layer is a spin-on first low k dielectric layer and said low k CMP protective
layer is a spin-on low k CMP protective layer.

49. The method of claim 48, wherein said spin-on low k CMP
25 protective layer has fine and evenly dispersed pores.

50. The method of claim 32, wherein said CVD hardmask/CMP
polish stop layer is a conventional CVD hardmask/CMP polish stop layer.